ES91r Summative Report - Electronics Design for an Atmospheric Chemistry Instrument - Anderson Research Group

Liam Mulshine

May 2017

1 Introduction

This semester I worked with the Anderson Research Group on a student led project funded by NASA to design and develop an atmospheric chemistry instrument to detect HCl and Ozone concentrations in the stratosphere. This instrument will be flying on one of NASA's weather balloons in mid-August above the mid-Western United States, collecting data that will contribute to the effort to determine the cause of Ozone depletion both over the continental US and across the globe.

As the only electrical engineering student on the team, I focused predominantly on two key electronic subsystems within the instrument: detection and power distribution. I was challenged to improve three instrument parameters: (1) the response time of the detection subsystem's electronics, (2) the overall signal-to-noise ratio and (3) the detection subsystem's power efficiency. I began the semester researching IR detection methods, and experimenting with two high-sensitivity IR detectors, looking for a solution to the slow response time and low signal-to-noise ratio of the detector subsystem in its current design stage. After comprehensive testing, I determined that the detector itself performed poorly at high frequencies, and was the central cause of the overall detection subsystem's slow response time. Further experimentation led me to the conclusion that the detector's response time improved with increasing temperature, while it's signal-to-noise ratio degraded. Since the detector temperature can be directly regulated with a built-in thermoelectric cooler, I determined with the engineers in the lab that, with proper control circuitry, we could selectively trade off between high SNR and small response time when necessary. Concurrently the team began noticing high levels of electrical noise coupling from the computer system into the detector circuitry. To address both of these findings, I designed a digitally and manually adjustable, low-noise, isolated power regulation board for the detection subsystem.

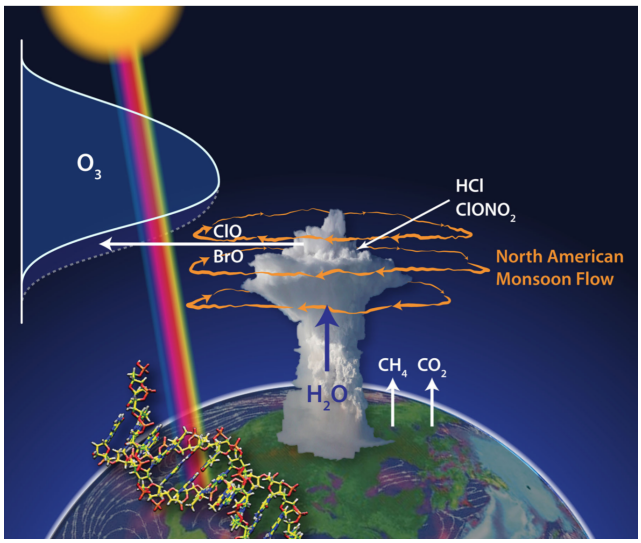
2 Project Motivation and Scientific Background

The cause of Ozone depletion has been a major focus within the field of atmospheric chemistry for the past few decades. While major strides have been made towards restoring the Ozone layer starting with the Montreal Agreement in the late 1980s, Ozone depletion continues in certain regions of the globe, including above much of the central United States.[1] Considering that a 1% reduction in the Ozone layer could lead to over 100,000 additional incidents of skin cancer across the globe, Ozone depletion continues to be a concerning trend.[2] Determining its cause is, thus, a pressing scientific challenge.

The Anderson Research Group has taken on this challenge and has developed considerable expertise in the matter. After joining the team, I first worked to develop an understanding of the scientific basis for the project. A central hypothesis developed by the Anderson Research Group underlying our experiment involves the relationship between climate forcing and stratospheric water vapor concentration and the effect of this relationship on catalytic Ozone depletion. An influx of high intensity storms above the central United States has increased the frequency of convective water vapor injections into the lower stratosphere, a region which is typically quite dry. Coupled with the North American Monsoon Flow during the summer months, the result is an environment of unusually high water vapor concentration in the lower stratosphere. Higher water particulate concentration is conducive to radical Chlorine formation, which has been shown to induce catalytic Ozone destruction. Below is a visual representation of the proposed chemical and meteorological processes forcing Ozone depletion.

[1] "The Montreal Protocol on Substances That Deplete the Ozone Later." Ozone Secretariat. N.p., n.d. Web. 01 May 2017.

[2] Anderson, James. March 2017. In class discussion.



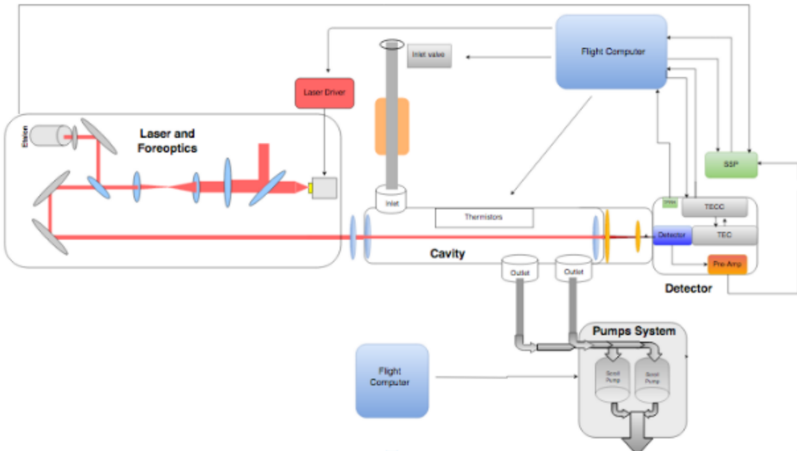
https://phys.org/news/2012-07-link-climate-ozone-loss-skin.html

3 Instrument Overview

The team has designed two instruments to detect HCl and Ozone respectively. Each utilizes the Integrated Cavity Output Spectroscopy (ICOS) method for detection, which takes advantage of the absorptive properties of each molecule to infrared light of distinct known values [3].

During my work with the Anderson Research Group, I focused predominantly on the detector subsystem for the HCl instrument, whose system diagram is shown below.

[3] E.J. Moyer, D.S. Sayres, G.S. Engel, J.M.St. Clair, F.N. Keutsch, N.T. Allen, J.H. Kroll, J.G. Anderson, Design considerations in high-sensitivity off-axis integrated cavity output spectroscopy. Phys. B 92, 467 (2008)



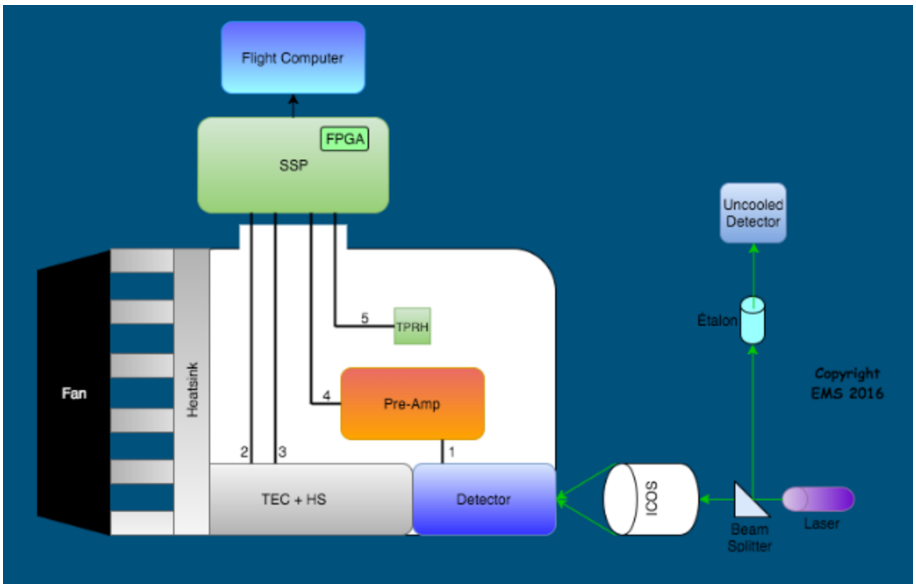
The system diagram provides a general outline of how each subsystem within the instrument interacts. The Laser Driver, highlighted in red, controls an IR laser source whose beam passes through a fore-optical stage before entering into the sample cavity. Both ends of the cavity are bounded by precisely aligned highly reflective mirrors, which are used to repeatedly reflect the laser beam to produce an effective laser path length of approximately 5 kilometers. As the beam passes through the cell, certain atmospheric species, dependent upon the beam's wavelength, absorb part of the incident light, before the beam exits the cell and hits the detector. Since we can precisely control the wavelength of light that enters the sample cavity with the Laser Driver, and since the absorbance spectra of HCl and Ozone are very well known, we can deduce the concentration of each species using the Beer-Lambert Law, comparing the signal intensity of the input beam with that of the output beam.

Despite the use of a high power input laser, the expected output signal from the ICOS cavity is not expected to exceed 10uW. Additionally, considering that the expected HCl concentration in the region is 50 pptv, the differential signal strength is expected to be quite small as well. Consequently, low-noise electronic design was critical to raise the signal above the noise floor and ensure measurement integrity.

4 My Research Project

Throughout the semester, I focused predominantly on the electronics associated with the detector subsystem. This subsystem, outlined in the figure below, converts the IR light signal from the ICOS cavity into an electronic signal. A preamplifier filters and amplifies the signal, before the Scalable Signal Process-

ing (SSP) board brings it into the digital realm for data storage within the flight computer.



One key element of the detector subsystem is the thermoelectric cooler and heat-sink (TEC + HS). After considerable experimentation with the IR detectors of interest, proper thermal tailoring was determined to be crucial in assuring high signal strength and fast response time.

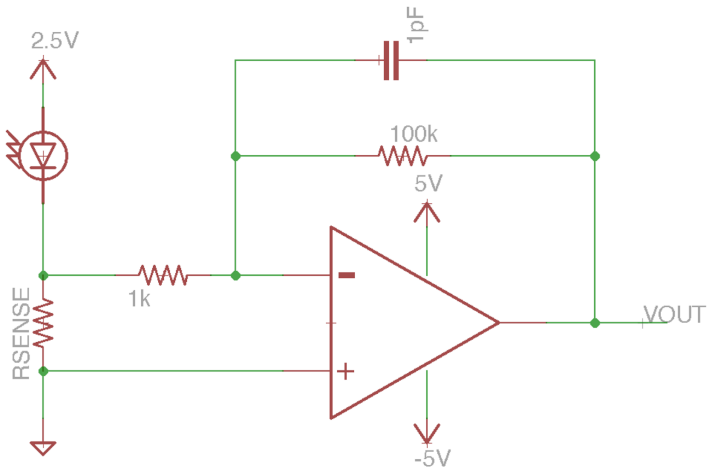
We utilize a Mercury Cadmium Telluride (MCT) infrared detector to convert the light signal of interest from the ICOS instrument into an electronic signal. The MCT detector is highly responsive at the wavelength of interest (3.375 microns), and has a detection area that is larger than most other highly sensitive IR detectors on the market (2 square mm) at the wavelength of interest. Large detection area is an important characteristic, due to the uncollimated nature of the laser signal that is output from the ICOS cavity. Were the detection area any smaller, only a portion of the output signal could be detected and, thus, the signal level would diminish.

The MCT detector specifications claimed a sufficiently fast response time; however, in practice, the response time was not nearly fast enough for our instrument. Since we expect an overall cavity response time of 17-21 us, we required the response time of the detector and electronics to perform at least an order of magnitude better. To produce accurate tests, calibration procedures and measurements, we required a response time between 1 and 2 us. While the claimed response time of the detector met this requirement, our testing demonstrated a response time of greater than 20 us, far off from what we desired.

I was challenged to find the cause of this slow response time, as well as a potential remedy. To do so, I took three distinct approaches. First, I worked with Marco Rivero, the lead electrical engineer in Anderson Research Group, to help design a low impedance input amplification stage for the high precision preamplification signal board on the instrument, under the assumption that the detector's parasitic capacitance was limiting the bandwidth of our signal. While this achieved an increase in response time by a factor of 2, the result was not sufficient for our purposes. Next, I worked to find the source of any parasitic capacitance that could be limiting the system's bandwidth; however, after running comprehensive tests on both the preamplification signal board, and the detector itself, I determined that neither component was a significant source of parasitic capacitance. Lastly, after a conversation with Marco and David Sayres, one of the lead researchers within the Anderson Group, I decided to look into the effect of temperature on the detector's response time, expecting cooler temperatures to improve the response. To the team's surprise, I found a clear inverse relationship between temperature and response time. This result led us to reconsider how we should control the detector temperature during flight and calibration, and was a key motivation for my design of a TEC controller to allow either manual or digital adjustment of the detector temperature.

5 Input Amplification Stage

After speaking with Marco about the detector subsystem's slow response time, we designed a low impedance input gain stage that, given our hypothesis about the capacitive nature of the detector sensor, would improve the system's response time to the desired level. The schematic design of the redesigned input stage is shown below.

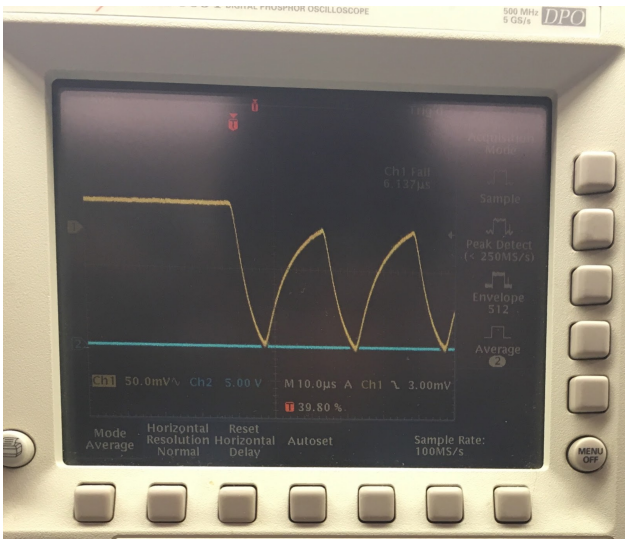


The IR photodetector at the top left of the schematic generates a current signal that is proportional to the intensity of 3.375 micron light incident on the detector. The RSENSE shunt resistor is used to convert the current signal into a voltage signal, which the inverting amplifier amplifies with gain of 100. The 1pF capacitor within the feedback loop limits the amplifier's bandwidth to

$$BW = \frac{1}{2\pi RC} = 1.6MHz$$

which exceeds the desired 1 MHz detector bandwidth and, thus, mainly serves to ensure output stability in the presence of higher frequency noise. RSENSE is typically low impedance, designed to be 1 ohm. Consequently, any parasitic capacitance inherent to the detector would see only 1 ohm in its path to ground, making any parasitic time constants negligible.

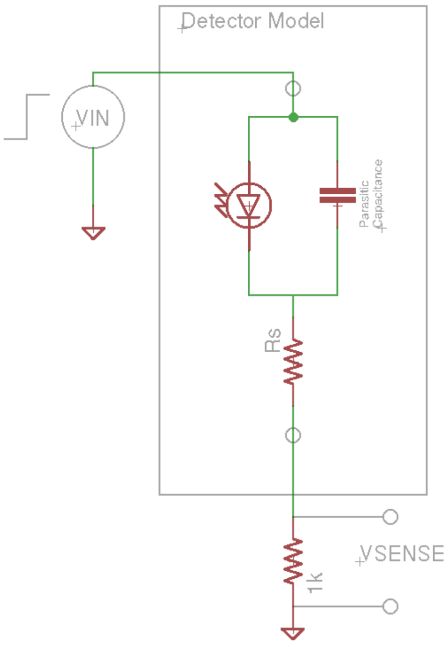
I tested the design in two different ways. First, I replaced the photoconductive detector with a fixed resistor, and simulated the detector signal with a 1MHz sine wave from a function generator, which I knew to have little inherent parasitic capacitance. The purpose of this test was to verify that the response time of the circuit itself met our specifications. The initial test indicated that I needed to reduce the bandwidth limiting capacitor to 1pF as shown in the schematic above; however, after this change, this test allowed us to confirm the fast response time of the detector input amplification stage circuitry. Next, I tested the circuit with the photodetector reinstalled. I utilized a TV remote as the IR signal source, and recorded the detector's response to the square wave signal that the TV remote emitted. Below is an oscilloscope reading of the detector signal immediately after the input gain stage.



Clearly, the signal is no longer a square wave, indicating that the subsystem has some bandwidth limit below what we desired. While the rise time had improved to 10 us, the improvement was insufficient to meet the system requirements that we defined. Consequently, I determined that it was necessary to work to develop a more complete understanding of the detector through experimentation, so that a new solution to the slow response time could be found.

6 Detector Analysis

After analyzing the response time of the input gain stage with no photodetector installed, I determined that the parasitic capacitance of the amplifier circuitry itself was negligible. Thus, if capacitance was the source of the overall subsystem's slow response time, it must have been present in the detector itself. I decided to isolate the detector from the rest of the system and analyze its step response. First, I developed a mental model of the detector with added parasitic capacitance and shunt resistance, which I have shown below connected to a test setup that I designed.



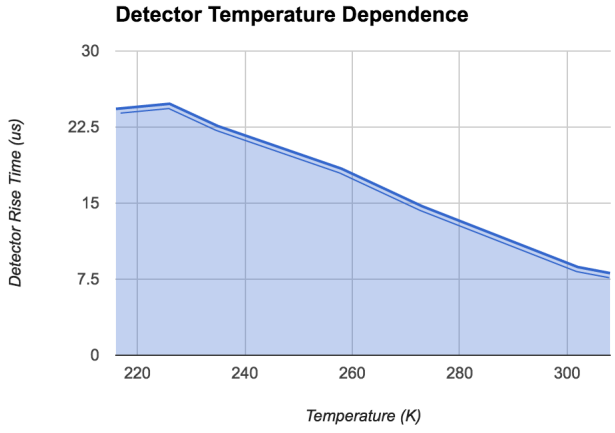
In this model, an ideal photoconductive detector is shown with parallel parasitic capacitance and series parasitic resistance (Rs). I determined that if a step input is applied to the upper terminal of the detector, the voltage, VSENSE, would step up to approximately VIN, before discharging to a steady state value

determined by the ratio between the 1k sense resistance and the series resistance of photodetector and shunt resistor. The detector resistance is typically around 1k under ambient light conditions, and Rs is orders of magnitude smaller, so I expected a steady state VSENSE value of VIN/2.

While VSENSE did reach a steady state value of VIN/2, there was no apparent initial jump to VIN. Instead, the sense voltage rose immediately to VIN/2. Thus, I was able to conclude that parasitic capacitance was not a central player in the slow response time of the detector subsystem.

After reporting my findings to the engineers and scientists in the Anderson Group, I spoke with Marco Rivero and David Sayres about possible next steps. We determined that it would be informative to explore how the response time varied under different environmental conditions, specifically under temperature variations. We hypothesized that cooler temperatures would improve the sensor's response time. Consequently, if we could develop a way to cool the detector below the temperature that the currently installed TEC was capable of setting, we could reduce the response time of the detector to more acceptable levels.

I began to design an experiment to test how the detector's response time changed with temperature. Utilizing an adjustable DC power supply, I controlled the power applied to the detector's internal thermoelectric cooler to directly adjust the temperature down from around room temperature to just under -60°C. Below are my results.



To our surprise, there was a clear inverse relationship between temperature and response time. The detector responded much faster at temperatures just above room temperature than it did at lower temperatures. Unfortunately, there was a trade-off: faster response time reduced signal-to-noise ratio. While this was

not the result that we expected, it was extremely informative, and gave us a clear method to directly control detector response time should we need to.

7 Engineering Challenge

While I was exploring the behavior of the MCT detector within the instrument, one of my peers noticed an influx of 1 MHz electrical noise on the instrument's analog ground plane whenever the instrument's computer system was powered on. This electrical noise was coupling into the detector signal, significantly reducing signal integrity. After speaking with Marco, we determined that it was necessary to isolate the detector power supply from that of the rest of the instrument. In addition, to address the temperature dependence of the detector, I would work to design an adjustable power supply, capable of powering a thermoelectric cooler to directly regulate the detector temperature.

7.1 Specifications

The first step in the design process for this power management board involved developing a list of specifications to which I could refer throughout much of the project. Specifications tables for both the preamplifier and TEC supplies are included below.

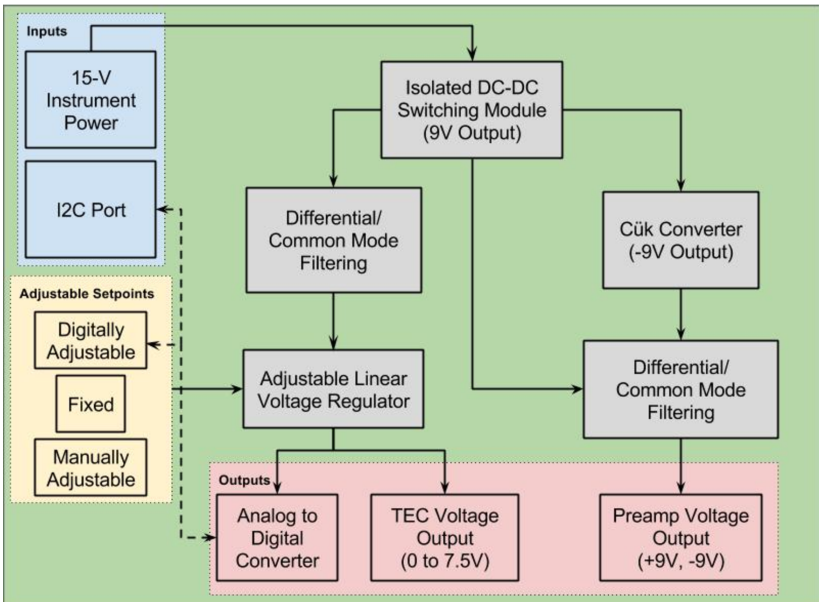
Preamplifier Supply Specifications	**Value**
Output Voltage	Fixed, Isolated: +9V, GND, -9V
Power Rating	3 W
Current Rating	150 mA

Thermoelectric Cooler Supply Specifications	**Value**
Output Voltage	Adjustable, Isolated: 0V to 7.5V
Adjustment Method	Manual, Digital, Fixed (Selectable)
Power Rating	4.5W
Current Rating	560 mA

We required galvanic isolation between the central instrument power supply and the preamp and TEC supplies in order to reduce the effect of noise from the flight computer on the detector signal as much as possible. The thermoelectric cooler supply needed to be adjustable, both manually and digitally so that it could be used to control the detector temperature both in the lab, and during flight. In addition, the thermoelectric cooler required current limiting, to protect against TEC overcurrent failure.

7.2 Block Diagram

The next step I took was to develop a block diagram of the overall system. Although this process was iterative, I have provided the final version below.



On the left, highlighted in blue are the inputs to the power supply board. Power is taken from the 15V supply on the instrument, and an I2C port is included to allow for direct digital control of the TEC supply voltage. The 15V instrument supply passes through an Isolated DC-DC Switching Module that generates a fixed, isolated +9V output. This isolated +9V output branches off to power the circuitry that generates the fixed preamp and adjustable TEC supply voltages on the power supply board.

The TEC supply stage can be located on the left branch of the block diagram after the Isolated DC-DC Switching Module. The isolated 9V supply is first passed through a differential and common mode filtering stage to attenuate any output ripple generated by the DC-DC switcher. This filtered supply is then passed through an adjustable linear voltage regulator, which I designed with overcurrent protection and an output range capable of extending down to 0V. This adjustable supply can be controlled by adjusting the regulator's voltage set-point either manually, or digitally via I2C communication with a digital-to-analog converter. An analog-to-digital converter provides feedback to the flight computer about the TEC supply voltage, and the supply voltage output, highlighted in red, is made directly accessible to the TEC on the back of the power supply board.

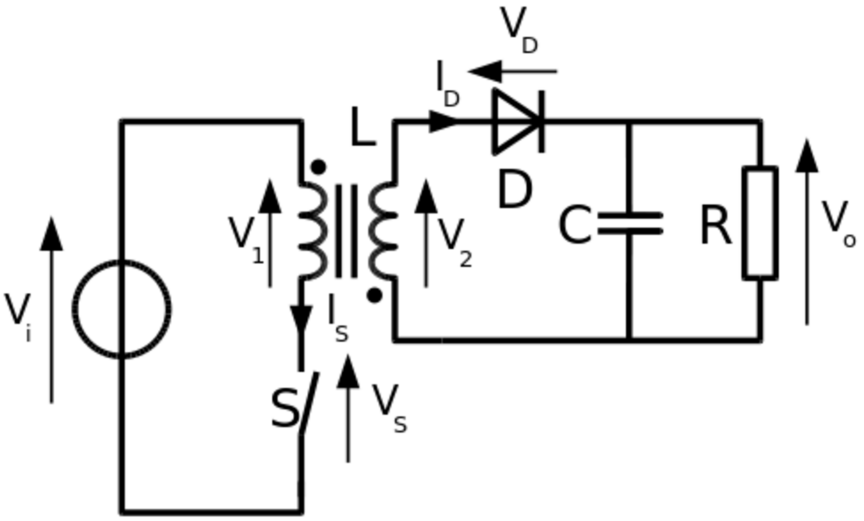
The preamplifier, alternatively, requires a dual-supply voltage (+9V, GND, and -9V). Using a Cük converter, I was able to generate the required negative supply rail. The Cük converter takes in a positive supply voltage and generates its inverted equivalent utilizing a capacitor to store energy between switching cycles. The +/- 9V supply is then passed through a differential and common mode filtering stage before being passed to the output.

8 Major Design Decisions

With a general block diagram designed, I began developing a more precise schematic design of the power supply circuitry. I will outline the design process I went through for 4 major subsections of the power module subsystem: the wide output range linear regulator, differential and common mode filtering stages, Cük converter selection and DC-DC switching module selection.

8.1 DC-DC Switching Module

The specification that perhaps held the most weight in this power supply design was its galvanic isolation. As explained earlier, isolation was deemed necessary to reduce the effect of noise from the flight computer on the detector signal. Indeed, many isolating DC-DC switching topologies exist, but one of the most common is the flyback converter. The isolated flyback topology achieves galvanic output isolation utilizing a transformer. Below is a schematic of a basic flyback converter.



https://commons.wikimedia.org/w/index.php?curid=691638

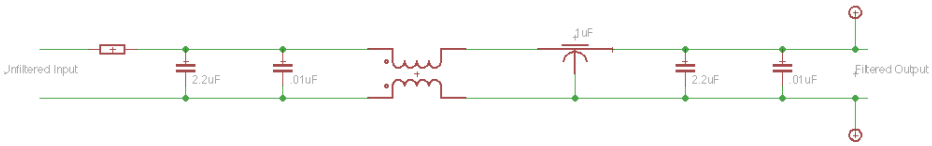
When switch, S, is closed, current flows through the primary winding, where energy is stored. When the switch it later opened, the diode, D, on the secondary side becomes forward biased since the secondary transformer winding has a polarity opposite the first, and current is either stored in the output capacitor or transferred directly to the load. Provided feedback, a controller can control the switch, S, to set the output voltage (the voltage across the output capacitor) to some known voltage with high precision and with approximately 80 percent efficiency - much more efficiently than with a simple linear regulator.

My first approach towards developing an isolated DC-DC switching supply was to design a switching converter utilizing a flyback converter integrated circuit (IC). After researching different flyback converter ICs, I narrowed my selection down to the LT3573, capable of generating both positive and negative output supplies and sourcing/sinking up to 1.25A. I also researched complete isolated DC-DC switching modules, and found one such component that met the specified power and output voltage specifications that I had defined: RECOM Power's REC7.5 Series switching module. Before moving forward, I felt that it would be beneficial to test and compare both options before designing the final PCB. I developed a breadboard prototype of the flyback topology with the LT3573 switching converter controller. While I was capable of generating a fixed output voltage with the design, the supply was very noisy and unstable with loads greater than half of an amp. The REC7.5 supply, in contrast, generated a clean, stable output voltage up to its specified maximum power output of 8W. While the flyback converter could allow us to generate both single and dual supply outputs provided that each external component was precisely tuned for

stable operation, the RECOM module seemed much more effective and dependable, especially given the time constraints of the project. Therefore, I decided to move forward with the reliable RECOM supply as the critical component that would ensure galvanic isolation between the input and output stages.

8.2 Differential and Common Mode Filtering

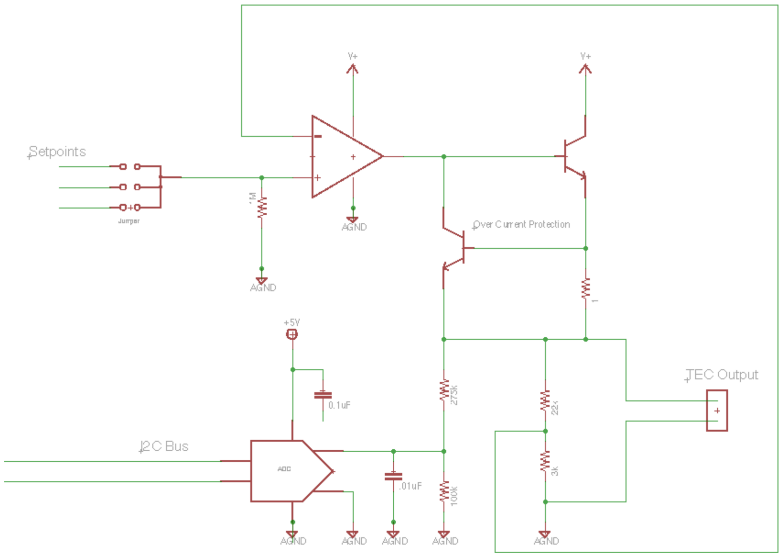
To further reduce noise levels on the preamplifier and TEC supply rails, I designed a multi-stage common mode and differential filter block. Below is the schematic design of the multi-stage filter.



The unfiltered input passes into the filter at the far left. This input passes through a ferrite bead which attenuates high frequency differential noise on the positive supply rail. The two parallel capacitors and common mode choke reduce the effect of common mode noise. In operation, the common mode choke attenuates common mode noise by mirroring any high frequency noise seen one transformer winding on the other transformer winding. While the absolute voltage (with respect to unfiltered ground) may change when noise passes through the system the relative voltage between the two terminals of the output end of the common-mode choke will stay approximately the same. The +9V rail from the common mode choke then passes into a feedthrough capacitor, which is designed to behave more like an ideal capacitor, achieving high insertion loss even at high frequencies. With additional bypassing, designed to respond to both high and low frequency noise, the supply is sufficiently filtered and ready for use.

8.3 Adjustable Linear Regulator

I designed an adjustable linear regulator with output range of 0-7.5V and overcurrent protection. While adjustable regulator ICs are quite common, none could be operated as low as 0V, while still meeting all other design specifications. Consequently I designed a regulator, whose schematic is shown below, that met all of our specifications.



This linear regulator uses feedback to set the output voltage to a level directly controllable by adjusting one of three user selectable setpoints. The user can move the position of a jumper to choose between fixed, manual, and digitally adjustable setpoints prior to operation. Once selected, the setpoint acts as the reference to an operational amplifier specified with rail-to-rail output operation. The output voltage is divided and fed back to this op-amp allowing direct control of the output with the user adjustable setpoint.

Careful consideration was made in selecting both the op-amp and output bipolar junction transistor (BJT). It was important to select a BJT with high current gain and low collector to emitter saturation voltage to ensure a wide output voltage range even under high load conditions. If the current gain was too low, the BJT might attempt to pull more base current than the op-amp could source under high load conditions, resulting in nonlinear operation. I selected the FTZ653 High Performance NPN Transistor, which boasts a high current gain of 175 at the expected maximum operating current of this linear regulator (560 mA). With such a high current gain, the maximum required base current is 3.2 mA, which falls well within the 20 mA maximum source current limit of the rail-to-rail op-amp I selected: the LMC6482.

The TEC used to control the detector temperature has a strict maximum current limit of 600 mA. Considering this, I designed an over-current protection stage at the output of the linear regulator. This consists of a small sense resistor, a second BJT and a negative feedback loop. In this simple yet effective current limiting scheme, a 1 ohm sense resistor is placed in the output current path of the regulator across the base-to-emitter junction of the current limiting transis-

tor. When the output current approaches 600mA, the voltage across the sense resistor approaches 0.6V, which is enough to turn the current limiting transistor on. This transistor limits the output current by "stealing" base current from the high current gain output transistor. As more output current is sourced, the base-to-emitter voltage of the current limiting transistor increases, causing more base current to be diverted from the output transistor, which effectively reduces the output current back to a reasonable level.

Lastly, I worked with Marco to select a 16-bit analog-to-digital converter, to provide feedback about the supply voltage level to the flight computer.

8.4 Cük Converter Selection

Since the preamplifier required a dual output supply voltage, I needed to design an inverting converter stage. After speaking about this with Marco, we determined that a Cük converter would perform the exact function we needed. Marco provided me with a power budget that he had generated for the preamplifier board when it was used on a previous instrument, which I used to determine exactly how much current would need to be sourced by the Cük converter. We settled on the LM2611 Cük converter, a converter that Marco had used on a past instrument and one that met the 150mA maximum current requirement of the preamplifier board.

9 Preliminary Prototype and Testing

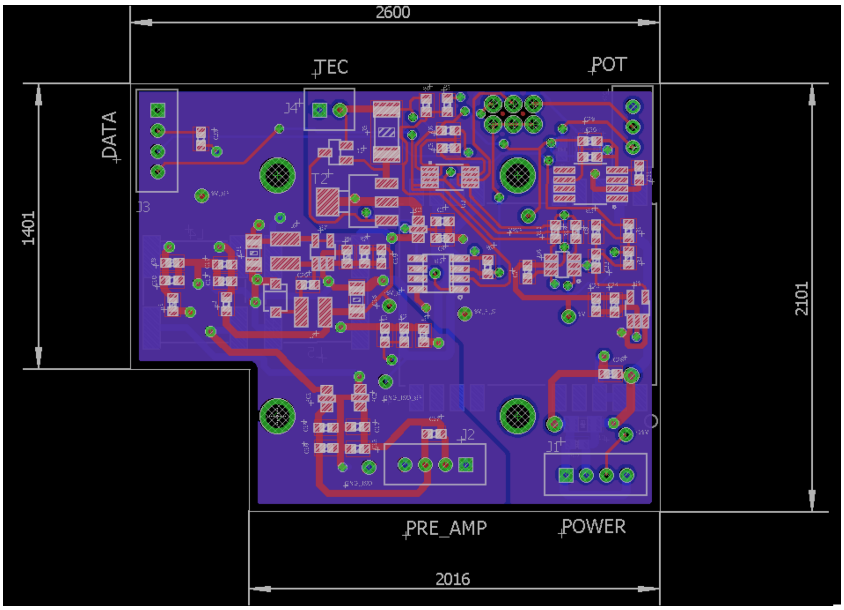
Before designing the final PC board layout, I tested each sub-circuit on a breadboard to ensure my core design would work. In particular, I wanted to verify how the circuit operated under maximum load conditions. I measured noise levels and their fundamental frequencies on the unfiltered supply lines, which I used in my differential and common-mode filter design. Specifically, I found that the Cük converter introduced 2.5MHz noise on the TEC and preamplifier supply lines, so I selected filter component values that achieved maximum insertion loss near 2.5MHz.

Both power supply outputs were stable at the maximum expected output current levels: 560 mA for the TEC supply and 150 mA for the preamplifier supply. Also, the isolating DC-DC switching module was stable under the maximum load condition: when both the TEC and preamplifier supplies were drawing maximum current.

10 Layout Design

After finalizing the schematic design with Marco and verifying its basic operation with a physical breadboard prototype, I began the layout design of the printed circuit board utilizing the Eagle CAD tool. The finalized version is

shown in the figure below.



I first considered the required geometry of the PC board. After speaking with Marco, we decided to design the board such that it could connect directly to the preamplifier board on the instrument. We analyzed the existing preamplifier setup and designed the board to plug directly into the preamplifier from the back side. We also aligned the board's 4 mounting holes with those on the preamplifier to ensure a simple and secure method for integration with the rest of the instrument.

After designing the board geometry, I began to consider component placement. When designing low noise power supply boards, careful consideration of current paths within the board is necessary. Therefore, it is important to place components such that current paths are short and isolated from other high current paths. While large component sizes and the PC board's unusual geometry complicated this effort, I did my best to separate the main subcircuits within the design and ensure that high current ground paths within the board were isolated from one another. The final iteration did not achieve perfect ground path isolation on the preamplifier supply; however, due to the lower current draw of this supply (less than 150mA), I expect that this will not affect noise levels substantially, if at all.

11 Testing the Final Prototype

The final PC board prototype is currently being fabricated and will soon be available for assembly and testing. I intend to have tested the board before I leave for the summer, to ensure that the design is ready for flight in mid-August. If production delays do not allow me to do this, I will keep in close correspondence with the Anderson Group over the summer months to ensure that the design is complete by the time of flight.

12 Conclusion

My experience with the Anderson Research Group this semester has been truly amazing, providing me with both research and engineering experience, working with a team of scientists and engineers on an open-ended multidisciplinary project. I would like to thank the entire Anderson Research Group for allowing me to contribute to this exciting project, and for supporting me along the way. In particular, I would like to thank Marco Rivero for sharing so much of his knowledge and time with me throughout the semester, and for his dedication to the project.