Preliminary Design of an Operational Transconductance Amplifier (OTA)

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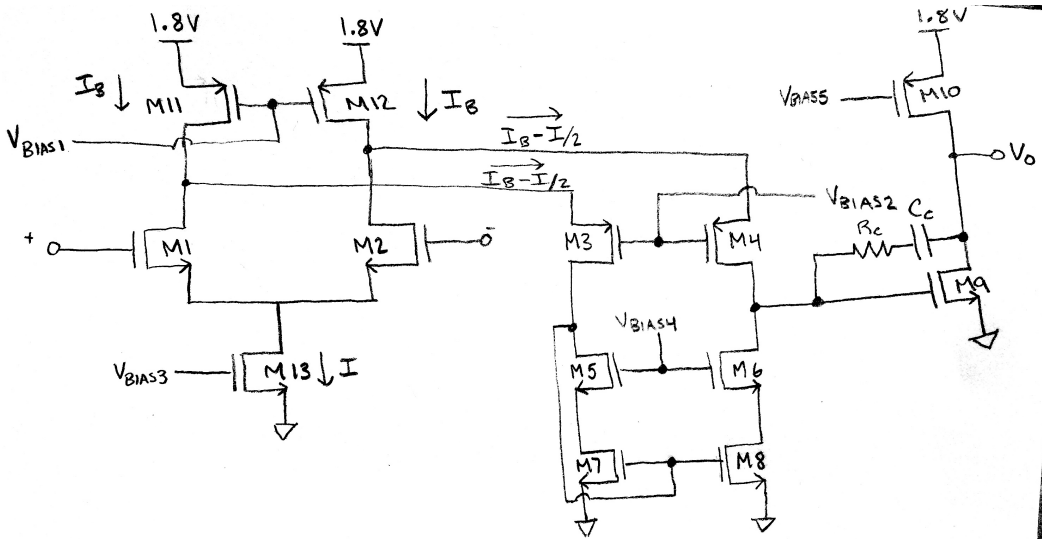
1 Schematic



After careful consideration of the design specifications for my OTA, I decided to use a 2-stage amplifier, utilizing a folded cascode first stage and a common source output stage. As I will show in this report, preliminary calculations suggest that this topology should meet all of the design specifications.

2 DC Operation

First, note that the following conditions hold for each transistor in my OTA

$$V_{DSsat} = 0.2V$$
$$V_{Th} = 0.5V$$

Also, note that I assume each transistor is operating with a $V_{OV} = 0.2V$, due to bandwidth, power consumption, and output swing considerations.

From these assumptions, I will analyze the DC operating conditions for my amplifier, and prove that each transistor in my amplifier will operate in the saturation region

when the input common-mode voltage and output voltage are both within their specified ranges.

2.1 Input Common Mode Voltage Range

The minimum V_{DS} for M13 is 0.2V since $V_{DSsat} = 0.2V$. Therefore the minimum common-mode input voltage at the input differential pair is $2V_{DSsat} + V_{Th}$, which equals 0.9V. Assuming the V_{OV} of M11 and M12 is 0.2V, the maximum input common-mode voltage is $V_{DD} - V_{OV11,12} + V_{th} = 2.3V$. Therefore, our specification that our OTA must be able to accept input voltages from 0.9V to 1.8V is met.

2.2 Biasing and Saturation

Since we have just one transistor on either end of both half circuits in the input differential pair, we should have enough headroom and legroom for all of the transistors in the input stage to remain in saturation, given that $V_{DSsat} = 0.2V$, as long as we appropriately bias the circuit.

The drain voltage of M1 and M2 is set by V_{BIAS2}. V_{BIAS2} must be small enough such that M11 and M12 can remain in saturation (V_{BIAS2} must be smaller than ~0.9V). Since I will assume $V_{BIAS2} \geq 0V$, M1, M2 and M13 should have enough room to remain in saturation, since a $V_{BIAS2} = 0V$ and $V_{OV} = 0.2V$ for M3 and M4, will cause the drain voltage of M1 and M2 to be at 0.7V, leaving more than enough room for the minimum V_{DS} of 0.2V for M13, M1 and M2.

We should set V_{BIAS2} to $V_{DD} - V_{OV12} - V_{SG4} = 1.8V - 0.2V - 0.7V = 0.9V$ so that M12 is operating at the edge of saturation, allowing the output swing of the folded cascode gain stage to go to 1.4V. Since I used a Wide-Swing Current Mirror Load, the output swing of my first gain stage can dip as low as $2V_{OV} = 0.4V$, while keeping M5, M6, M7, and M8 in saturation. This is only possible if $V_{BIAS4} = V_{th} + 2V_{OV} = 0.9V$. This allows the drain voltage of M5 to dip as low as 0.7V (in order to keep M5 and M7 in saturation), and as high as 1.4V (in order to keep M3 and M11 in saturation).

As I have just explained, it will be possible to keep all of the transistors in my first folded-cascode gain stage in saturation for an input voltage range of 0.9V to 1.8V.

Now I will show that all transistors in my second gain stage will remain in saturation.

First, let me clarify that, although the output voltage of the first stage could dip as low as 0.4V, while keeping all transistors for the first stage in saturation, the second common source gain stage requires that this output voltage not dip below 0.7V, so that M9 can operate at an overdrive voltage of 0.2V. If this is true, then V_O of the second gain stage can dip as low as 0.2V. Additionally, assuming that the overdrive voltage of M10 is 0.2V, V_O of the second gain stage can jump as high as 1.6V, while

ensuring that all transistors are in saturation. Therefore, since the output voltage of the second stage corresponds to the output of my operational transconductance amplifier, I would expect the full output swing of my amplifier to be $0.2V < V_O < 1.6V$, which satisfies the output swing specifications for this project.

3 Small Signal Operation

At this point we need to determine what the gain of our amplifier will be. The folded cascode amplifier topology has approximately infinite input resistance, a transconductance $G_m = g_{m1} = g_{m2}$, and an output resistance, R_o. Therefore the gain of the first stage of my OTA is

$$A_v = G_m R_o$$

Due to the symmetry of the circuit, you can make a half-circuit analysis of the folded cascode amplifier to determine its small signal DC gain. The output resistance of the folded cascode first stage is the parallel output resistance of the folded cascode amplifier and the cascode current mirror's output resistance. The output resistance of the folded cascode amplifier, R_{o1} is the parallel output resistance of M2 and M4 scaled by the small signal gain from M4:

$$R_{o1} = (g_{m4} r_{o4})(r_{o2} || r_{o12})$$

The output resistance of the cascode current mirror, R_{o2}, is the output resistance of M8 scaled by the small signal gain from M6:

$$R_{o2} = (g_{m6} r_{o6}) r_{o8}$$

Thus,

$$R_o = R_{o1} || R_{o2} = \{(g_{m4} r_{o4})(r_{o2} || r_{o12}) || (g_{m6} r_{o6}) r_{o8}\}$$

and, then

$$A_v = g_{m1}\{(g_{m4} r_{o4})(r_{o2} || r_{o12}) || (g_{m6} r_{o6}) r_{o8}\}$$

which is on the order of $(g_m r_o)^2$, and thus can be approximated as such.

The second gain stage serves the purpose of extending the output voltage swing of my OTA. However, it too will have a gain

$$A_v = g_{m9}(r_{o9} || r_{o10})$$

In order to determine the transistor sizes for my amplifier, I will consider each stage separately.

4 Transistor Sizing

Starting with the minimum L of 180nm, I will work to find the width and bias current of the transistors in the first gain stage.

4.1 M1 and M2

Setting $f_t = 10GBW = 50MHz$, yields a current density $\frac{I_D}{W} = 10^{-7}\,\frac{A}{um}$, which puts the transistor in the sub-threshold region. Therefore, I will choose $V_{OV} = 0.2V$, which pushes the bias current up to $\frac{I_D}{W} = 5\ x\ 10^{-5}\ \frac{A}{um}$. This corresponds to an f_t of approximately $10^{10}MHz$ which far exceeds the requirement that $f_t = 10GBW$. This current density yields an intrinsic gain of ~40 V/V, so I would expect my initial stage to yield a total gain of $\sim (40)^2 = $ 1,600 V/V.

The current density found above yields a $\frac{g_m}{W} \cong 3x10^{-4}$. We know that $g_{m1} = (GBW)(C_c)$, where GBW = 50MHz, and $C_c = \frac{C_L}{2} = 5pF$. Therefore, our expected $g_{m1} = 1.57x10^{-3}$. From this we can find the width (W) of M1 and M2 (assuming M1 = M2).

$$W = \frac{g_{m1}}{\frac{g_{m1}}{W}} = \frac{1.57x10^{-3}}{3x10^{-4}} = 5.24um$$

$$I_D = \left(\frac{I_D}{W}\right)(W) = 264uA$$

4.2 M3 and M4

I will set the drain current through M3 and M4 to be approximately 4 times smaller than that of M1 and M2, in order to try to make the output resistance of M3 and M4 large, and to reduce total power consumption. Thus, $I_{D3,4} = 6.6x10^{-5}A$.

I will set the overdrive voltage of M3 and M4 to approximately 0.2V in order to keep my transistors in saturation. Choosing L = 540nm, $\frac{I_D}{W} \cong 2uA$, since M3 and M4 are p-channel MOSFETS. Thus

$$W = \frac{I_{D3,4}}{\frac{I_D}{W}} = 32.75um$$

4.3 M5, M6, M7 and M8

I will assume that M5, M6, M7, and M8 operate at the same overdrive voltage of 0.2V. Also, note that $I_{D3,4} = I_{D5,6,7,8} = 6.6x10^{-5}A$. For an n-channel MOSFET with L = 540nm, the current density, $\frac{I_D}{W} = 2x10^{-5}A$. Thus,

$$W = \frac{I_{D5,6,7,8}}{\frac{I_D}{W}} = 3.3um$$

4.4 M11 and M12

The current through M11 and M12 is the $I_{D3,4} + I_{D5,6,7,8} = 328uA$. Assuming an overdrive voltage of 0.2V, and L = 540nm, and also given that M11 and M12 are p-channel MOSFETS, the current density, $\frac{I_D}{W} = 2uA$. Therefore,

$$W = \frac{I_{D11,12}}{\frac{I_D}{W}} = 164um$$

4.5 M13

The current through M13 is $2I_{D1,2} = 528uA$. For an n-channel MOSFET with overdrive voltage of 0.2V and L = 540nm, the current density, $\frac{I_D}{W} = 2x10^{-5}\frac{A}{um}$, and, thus

$$W = \frac{I_{D13}}{\frac{I_D}{W}} = 26.2\ um$$

4.6 M9

For the second gain stage, we must take into account how the compensation capacitor C_C affects the second pole of the amplifier, and, thus, the value of g_{m5}. We know that $w_{p2} = \frac{3g_{m5}}{4C_L}$, $|w_{p2}| = 1.5GBW$, and $GBW = \frac{g_{m1}}{C_c}$. Thus, $g_{m5} = 4g_{m1}$.

For an n-channel MOSFET with L = 540nm, and an overdrive voltage of 0.2V, the current density, $\frac{I_D}{W} = 1x10^{-5}A$, yielding an intrinsic gain of 200. The expected $\frac{g_m}{W} = 8x10^{-5}$, and from the expression above, $g_{m5} = 4(1.57x10^{-3}) = 6.28x10^{-3}$. Thus,

$$W = \frac{g_{m5}}{\frac{g_m}{W}} = 78.5um$$

$$I_D = \left(\frac{I_D}{W}\right)(W) = 0.785mA$$

4.7 M10

For a p-channel MOSFET, with overdrive voltage of 0.2V and L = 540nm, the current density, $\frac{I_D}{W} = 2\frac{uA}{um}$. Since $I_D = 0.785mA$,

$$W = \frac{I_D}{\frac{I_D}{W}} = 392.5\ um$$

5 Power Budget

Since I will need at most 5 separate current bias transistors, assuming that at most 10uA will flow through each, $P_{BIASING} = (10uA)(1.8V)(5) = 0.09mW$.

Also, $P_{amplifier} = (1.8V)(I_{M10} + 2I_{M12}) = 2.59mW$.

Therefore, the total power consumption of my amplifier with biasing is

$$P_{TOT} = P_{BIASING} + P_{amplifier} = 2.68mW$$

This is less than 3mW, so my design satisfies the power specifications for the OTA.

6 Gain Bandwidth Product

Since $GBW = \frac{g_{m1}}{C_c}$, the gain-bandwidth-product of my amplifier should be set at 50MHz, especially considering that the current density in each transistor in my amplifier is high enough such that the unity gain frequency for the transistor is greater than 10 times the gain-bandwidth product. As proof, the current density for an n-channel MOSFET needs to be greater than approximately .3uA in order to achieve an $f_t > 10GBW$, which is the case for all transistors in my amplifier. For a p-channel MOSFET, the current density must be greater than 1uA, which is also met by all of the p-channel MOSFETs in my amplifier. Thus, I would expect a GBW = 50MHz, as I designed for.

7 Compensation Resistor

We know

$$w_Z = \frac{1}{C_C\left(\frac{1}{g_{m5}} - R_C\right)} < 0$$

and

$$w_Z > \left|w_{p2}\right| = (1.5)GBW = \frac{1.5g_{m1}}{C_C}$$

Thus,

$$\frac{1}{g_{m5}} < R_C < \frac{1}{(1.5)g_{m1}}$$

Since $g_{m5} = 6.28x10^{-3}$ and $g_{m1} = 1.57x10^{-3}$, $159\ \Omega < R_C < 425\ \Omega$.
Therefore, I will set

$$R_C = 291\ \Omega$$

8 DC Gain

Although the approximation of the gain for the first two stages, $A_V = (g_{m1}r_{o1})^2(g_{m5r_{o5}})$ gives me a rough estimate of my amplifier's gain, I wanted to more accurately estimate my amplifier's gain. To do so, I used the data in Table 3, which can be found in Section 10, and the full expressions for gain derived in Section 3.

I found that the gain of the first stage, $A_{V1} = 9160\frac{V}{V}$ and the gain of the second stage, $A_{V2} = 160\frac{V}{V}$, yielding a total amplifier gain of $A_{Vtot} = A_{V1}A_{V2} = 1{,}465{,}600\ V/V$. Which far exceeds the minimum gain required for my amplifier.

9 Phase Margin

We know,

$$Phase\ Margin = 90\ degrees - \tan^{-1}\left(\frac{f_t}{f_{p2}}\right)$$

where $f_t = GBW = 50MHz$ and $f_{p2} = (1.5)GBW = 75MHz$. Therefore,

$$Phase\ Margin = 90 - \tan^{-1}\left(\frac{1}{1.5}\right) = 56.3\ degrees$$

This is within the specification that $Phase\ Margin > 55\ degrees$.

10 Tables

Table 1

	Specification	Units	Result
Gain Bandwidth Product	50	MHz	50
Phase Margin	55	Degrees	56.3
Maximum Power	3	mW	2.68
Output Swing	0.25 to 1.55	V	0.2 to 1.6
DC small signal Gain	> 10 000	V/V	1,465,600
Input Voltage Range	0.9 to 1.8	V	0.9 to 2.3
Capacitive load	10	pF	10
Supply Voltage	1.8	V	1.8

Table 2

Device	W (um)	L (um)	DC Current
M1,M2	5.24	.18	264 uA
M3,M4	32.75	0.54	66 uA
M5,M6,M7,M8	3.3	0.54	66 uA
M11,M12	164	0.54	328 uA
M13	26.2	0.54	528 uA
M9	78.5	0.54	785 uA
M10	392.5	0.54	785 uA

Table 3

Device	Current Density (uA)	Device Type	Length (um)	Transconductance	Intrinsic Gain	Output Resistance (Ω)
M1,M2	50	N	0.18	3.E-04	50	1.67E+05
M3,M4	2	P	0.54	2.00E-05	200	1.00E+07
M5,M6,M7,M8	20	N	0.54	9.00E-05	200	2.22E+06
M11,M12	2	N	0.54	2.00E-05	200	1.00E+07
M13	20	N	0.54	9.00E-05	200	2.22E+06
M9	10	N	0.54	8.00E-05	200	2.50E+06
M10	2	P	0.54	2.00E-05	200	1.00E+07