Designing an Operational Transconductance Amplifier (OTA) in Cadence

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1 From Hand Calculations to Simulation

Rarely do preliminary hand calculations in amplifier design result in values that exactly match the values that produce acceptable simulation results. This can be attributed to the numerous approximations made in the initial design process, without which a preliminary design would prove very complicated, if not impossible. In my amplifier design, the devices that I ultimately used in simulation were similar in size to those that I initially calculated. However, a few key differences existed between my initial design and my simulated design.

2 Transistor Sizing and Biasing

Please refer to section 6 for a full schematic of my amplifier. Each transistor on the schematic is indexed (i.e. M1, M2, etc.), and I will use these indexes to reference specific transistors in my amplifier for convenience.

2.1 M1, M2

Sizing M1 and M2 was critical in my amplifier, since these transistors make up the differential input stage. Thus, the gain of the entire amplifier is strongly dependent upon the parameters of these devices. Upon an initial pass through of my design, I found that my gain was not quite as high as I would have hoped. It just barely met the specification of 10,000 V/V. Knowing that the gain was strongly dependent upon the transconductance of M1 and M2, I decided to try to increase g_m for these transistors. To do so, I considered that $g_m = \frac{2I_D}{V_{OV}}$. Since the current through each of M1 and M2 should be approximately constant (assuming saturation), due to the presence of the current source, M13, I realized that I would need to reduce V_{OV} in order to increase the transconductance. The only parameters that I was able to vary were W and L. Since $I_D = k_n \left(\frac{W}{L}\right) V_{OV}^2$, and since the drain current through M1 and M2 was constant due to the presence of M13, I realized that I could increase the width of the transistor to reduce the overdrive voltage. Doubling the width, W, reduced the overdrive voltage and increased the transconductance of M1 and M2 sufficiently, such that the gain of my circuit well exceeded the specifications. The tradeoff to this increase in gain was a slight reduction in bandwidth, which is a very common tradeoff in amplifier design. I had to be careful, however, not to increase the width of my input stage transistors so much so that it pulled the transistors into

the cutoff region, by reducing the gate to source voltage below the threshold level of the transistor.

2.2 M3, M4

M3 and M4 are the cascode transistors to the input differential pair, M1 & M2. The sizes that I calculated in my preliminary design matched fairly well to those of my final design.

In order to bias M3 and M4 I utilized the current mirror composed of M16 and M17, whose current is set by the transistor, M15 (which is biased by M14, whose current is set by a 10uA current reference). Transistor M17 in the current mirror sets the current through transistor M19. I diode connect M19 in order to force it into saturation, allowing me to adjust the value of W (fixing L at 540nm, which is longer than the input differential pair transistor lengths to ensure higher output resistance), in order to set the bias voltage to an appropriate value. Since the current through M19 is approximately fixed, increasing the width of M19 will reduce the bias voltage due to phenomenon of channel length modulation; in other words, the bias voltage is inversely proportional to the width of M19.

Ideally, the bias voltage would be high enough such that M11 and M12 are pushed to the edge of saturation (~0.9V), which would allow for a high swing at the output stage of the folded cascode amplifier. However, since we have a second common source gain stage at the output of the OTA, achieving the maximum output swing in the first stage is not particularly critical. Therefore, I decided to set the bias voltage of M3 and M4 to slightly lower than 0.9V, providing me with some leeway in choosing parameters for the other transistors in my circuit, while keeping all devices within saturation. However, I needed to make sure not to set the bias voltage too low, lest I reduce the drain voltage of M11 and M12 so much so that M3, M4, and the transistors that make up the cascode current mirror below M3 and M4 have difficulty staying saturation. Therefore, I set the bias voltage for these transistors to approximately 0.8V, by performing a DC analysis of the bias voltage while sweeping over the width of transistor M19.

2.3 M5, M6, M7, M8

Biasing and sizing these transistors was, at first, a bit tricky. However, ultimately, I ended up with transistor sizes quite similar to those that I had calculated initially. The difficulty here comes from the fact that the voltage at the drain of M5 (which is the same as the voltage at the gate of M7 and M8) must be at least $V_{thn} + 2V_{OV}$, given the high swing cascode topology. Thus, the widths of these transistors (assuming L = 540nm) must be small enough to allow the voltage at the drain of M6 to be high enough to keep the gate of the common source amplifier, M10, at a voltage greater than its threshold voltage. Additionally, the widths must be large enough to assure that M11, and M12 are in saturation. I was able to find a value of W that allowed for

me to achieve both requirements. Using the widths that I had initially calculated caused the voltage at the drains of M5 and M6 to be higher than I had initially desired. Since different bias voltages and the current sources above these transistors set the current through them, I determined that increasing these transistors' aspect ratios would reduce the voltage at the drain of M5 and M6, due to the effects of channel length modulation.

Appropriately setting the bias voltage at the gates of M5 and M6 is critical. In order to ensure that all transistors in the cascode current mirror are in saturation, this bias voltage must be at a minimum of approximately $V_{thn} + 2V_{OV}$. In order to set this voltage, I used the two transistors, M20 and M21. M21 is biased by M1 and the reliable 10uA current reference. Since the current through the diode connected transistor M20 is approximately fixed, assuming all devices are in saturation, I can alter the bias voltage as before by adjusting the width of transistor M20. After performing a DC Analysis and a sweep over the width of M20, I determined the value of W that would give me a bias voltage approximately equal to 1V. This would give me a bit of leeway in ensuring that M7 and M8 were in saturation.

2.4 M9, M10

The sizes of M9 and M10, which make up the 2nd gain stage, differed most from the sizes, which I initially predicted. This is likely due to the fact that a large amount of current flows through each, necessitated by the capacitive load at the output of this stage. Thus, any transistor device differences that I did not predict in the initial design phase were exaggerated.

I noticed that M9, which serves as a current source in this simple common source stage, was pulling more current than expected with the predicted 392um width. Although more current would likely help to increase the bandwidth of the amplifier, and help drive the 10pF load without instability, I had a power limit of 3mW, and a gain specification to meet, so I needed to reduce the drain current in this branch. In order to do so, I considered how the current through M9 is set. Essentially, a bias voltage is supplied to the gate of M9, using a current mirror configuration with M16. Since M16 is diode connected, the transistor is forced into saturation. Also, the current through M16 is set by the current source, M15, as explained above. Thus, the voltage necessary to pass the current set by M15 through M16 will appear at the gate of M16. In order to set the current through M9, I can alter its aspect ratio, since $I_9 = \frac{\left(\frac{W}{L}\right)_9}{\left(\frac{W}{L}\right)_{16}} I_{16}$ and I_{16} is fixed. Thus, to reduce the current through M9, which is what I needed to do, I reduced M9's aspect ratio, by lowering its width.

M10 also was quite different in simulation than expected. Since the current through M10 was fixed, set by M9 as explained above, the aspect ratio of the transistor needed to be set such that both M9 and M10 remained in saturation, but also such that the transconductance of M10 was within range of what I had calculated it to be,

since the gain of the amplifier is very dependent upon this g_m. A higher aspect ratio would attempt to force more current through M10, which, assuming ideal transistors with infinite output resistance, cannot be done, since the current is set by M9. However, if you consider channel length modulation in the transistors, which arises due to the finite output resistance characteristic of all practical transistors, you can modulate the drain current slightly by varying the drain to source voltage of the transistors. The relationship is direct; increasing V_{DS} will increase drain current. Thus, if we increase the aspect ratio of M10, causing M10 to work to pull more current, the drain voltage of M9 should reduce in an attempt to satisfy the needs of M10. However, this drain voltage is also the drain voltage of M10, so if the aspect ratio is increased so much so that the drain voltage drops below a lower limit, M10 will exit the saturation region, and, thus, wont operate as expected.

Since the gain of the second stage is dependent upon the transconductance of M10, I would, ideally, want g_{m10} to be high. To do so would require the drain current of M10 to be high, considering the relationship $g_m = \frac{2I_D}{V_{OV}}$, and that V_{OV} is set by the output of the first gain stage. I noticed that I did not have much of an ability to increase the drain current through M10, however, since doing so would reduce the drain voltage of M10 as explained before, thus pushing the transistor out of saturation. Yet, since the current set by M10 was higher than I had anticipated, I did not need to try to increase the drain current of M10 in order to achieve a transconductance value within range of what I had expected, resulting in a lower width for this transistor than I had initially calculated.

2.5 M11, M12

The current mirror load composed of M11 and M12 is, like M9, also biased by M16, which can be done since M9, M11, M12 and M16 are all pmos transistors with their sources tied to V_{DD}. Thus, to set the current through these transistors, I needed to determine the ratio of the aspect ratios of M9 and the transistors in the current mirror load. As before, M11 and M12 sourced more current than expected using the predicted values of W, so I reduced them slightly in order to get a current value closer to that which I had expected. I did not want to source a large current, since that would cause more current to flow through M3, M4, M5, M6, M7 and M8, and would effectively reduce their output resistance, and thus the gain of the circuit. It would also increase the power consumption of the circuit. I was able to set the aspect ratios of M11 and M12 to approximately achieve the current that I had designed for.

2.6 M13

Appropriately sizing M13 is important since it affects how much current flows through each branch of the folded cascode amplifier. In order to consider how I set the width of this transistor, we need to consider how I biased it. The diode

connected transistor M14, supplies voltage to the gate of M13, in a similar way to how the diode connected transistor, M16, supplies bias voltages to other transistors in the circuit. The current through M13 is proportional to the ratio of the aspect ratios of M13 and M14, since the source of both transistors is connected to ground. In order to keep the output resistance of the current source, M14, low, which would help increase the accuracy of the current mirror, I made the width of this transistor small, and its length large. Then I determined the how wide I needed to make M13 in order for it to sink approximately 530uA. In practice, the width that I calculated was slightly higher than the width that got me the desired DC current/current density.

3 Amplifier Results

While designing my amplifier in the Cadence simulation tool, I came across various amplifier designs that met the specifications for this project. However, some designs met the specifications better than others. Here I will present the results that I achieved for the amplifier that I discuss in the majority of this report. However, I will also show the characteristics of an amplifier that I designed that demonstrates the tradeoff between gain and bandwidth in amplifier design quite well.

Note that to test if my amplifier met spec for the entire output swing of my amplifier, I tested the amplifier at the bottom and top of the output swing range: 250mV and 1.55V respectively. In general, for output voltages between these limits the DC gain and bandwidth results improved. The stability reduces slightly, but still met specifications.

3.1 DC Gain and Bandwidth

I met both the DC gain and bandwidth specifications for my amplifier. The DC gain was quite a bit lower than I had anticipated from my preliminary calculations. This is likely due to the many assumptions I made during the initial design process. Since the transconductance of my input differential pair transistors in the first stage, and the transconductance of the input transistor in the second common source gain stage are larger than the transconductances that I calculated by hand for these devices, I would imagine that the comparatively small gain is a result of output resistances that were smaller in simulation than in design.

I was able to meet the bandwidth specification for this amplifier with a compensation capacitor equal in value to the value that I calculated. However, knowing that the bandwidth is predominantly determined by the first pole frequency, I could adjust the value of C_C in order to adjust the location of the first pole. I know that there is an inverse relationship between w_{p1} and C_C; increasing C_C will decrease the value of the dominant pole frequency. Please see Figures 1 and 2 for the magnitude plot of my amplifier.

3.2 Phase Margin

I was able to meet the phase margin specifications in my amplifier design here with quite a bit of padding, suggesting that my amplifier is rather stable. Knowing that

$$Phase\ Margin = 90\ degrees - \tan^{-1}\left(\frac{f_t}{f_{p2}}\right)$$

I could increase the phase margin by reducing the unity gain frequency. In other words, drawing from the relationship between the unity gain frequency and the compensation capacitor value, I could increase the phase margin by increasing the capacitance of C_C. Please see Figures 1 and 2 for the phase plot of my amplifier.

3.3 Power Supply Rejection Ratio

The power supply rejection ratio that I achieved in my amplifier is acceptable. Power supply rejection ratio can be calculated as follows:

$$PSRR = -20\log\left(\frac{V_{out}}{V_{supply}}\right)$$

where V_{supply} is an unwanted AC signal on the power supply line, and V_{out} is the AC signal that appears at the output due to ripple on the power supply. It behaves as expected in my amplifier, with PSRR dropping off at high frequencies, due to the existence of parasitic capacitances in the transistors. Please see Figures 1 and 2 for the PSRR plot of my amplifier.

3.4 Common Mode Rejection Ratio

The common mode rejection ratio can be calculated as follows:

$$CMRR = -20\log\left(\frac{V_{cm}}{V_d}\right)$$

where V_{cm} is the AC output voltage of my amplifier due to the application of a common mode AC signal, and V_d is the AC output voltage of my amplifier due to the presence of a differential AC signal. This calculation assumes that the differential and common mode AC signals are identical. If they are not, then

$$CMRR = -20\log\left(\frac{A_{cm}}{A_d}\right)$$

where A_{cm} is the common mode gain, and A_d is the differential gain. The common mode rejection ratio of my amplifier is not exactly typical when operating at the upper and lower bounds of my output swing. However, it is rather high within the

specified bandwidth of my amplifier and, in general, falls off for high frequencies. Please see Figures 1 and 2 for the CMRR plot of my amplifier.

3.5 Gain Bandwidth Tradeoff

The tradeoff between gain and bandwidth in amplifier design is huge. Essentially, it refers to the (almost always) necessary tradeoff between DC gain and amplifier bandwidth when designing an amplifier: increasing gain tends to reduce bandwidth, and vice versa. In my design, I witnessed this tradeoff when testing different DC currents in my 2^{nd} gain stage: the common source amplifier. As I reduced the DC current in the second stage, the transconductance and output resistance of this stage increased, thus increasing the DC gain of the amplifier. However, the bandwidth reduced, likely due to the enhanced Miller effect associated with having a higher gain, which has the effect of reducing the gain-bandwidth product of the common source amplifier by amplifying the parasitic capacitance between the gate and the drain of the input transistor. The Magnitude, Phase, CMRR, and PSRR plots for the higher bandwidth amplifier are presented first, followed by those for the higher gain amplifier.

3.6 Input Voltage Range

Due to the nature of my test bench setup, I was unable to characterize my amplifier up to 1.8V: the maximum input voltage defined in my amplifier's specifications. This is due to the fact that the test bench that determines the systematic offset voltage of my amplifier cannot reach 1.8V while keeping both transistors in my output stage in saturation. Therefore, I was only able to characterize my amplifier's input voltage range up to 1.6V. I found that at 1.6V, I still met all required specifications for my amplifier. While the gain and gain bandwidth product reduced, the CMRR, PSRR and Phase Margin increased. In contrast, at the lower bound of my input voltage range, 0.9V, my gain increased, while my CMRR, PSRR and Phase Margin noticeably reduced, but remained within the specifications.

4 Figures

Figure 1: Higher Bandwidth Amplifier: Output at 250mV

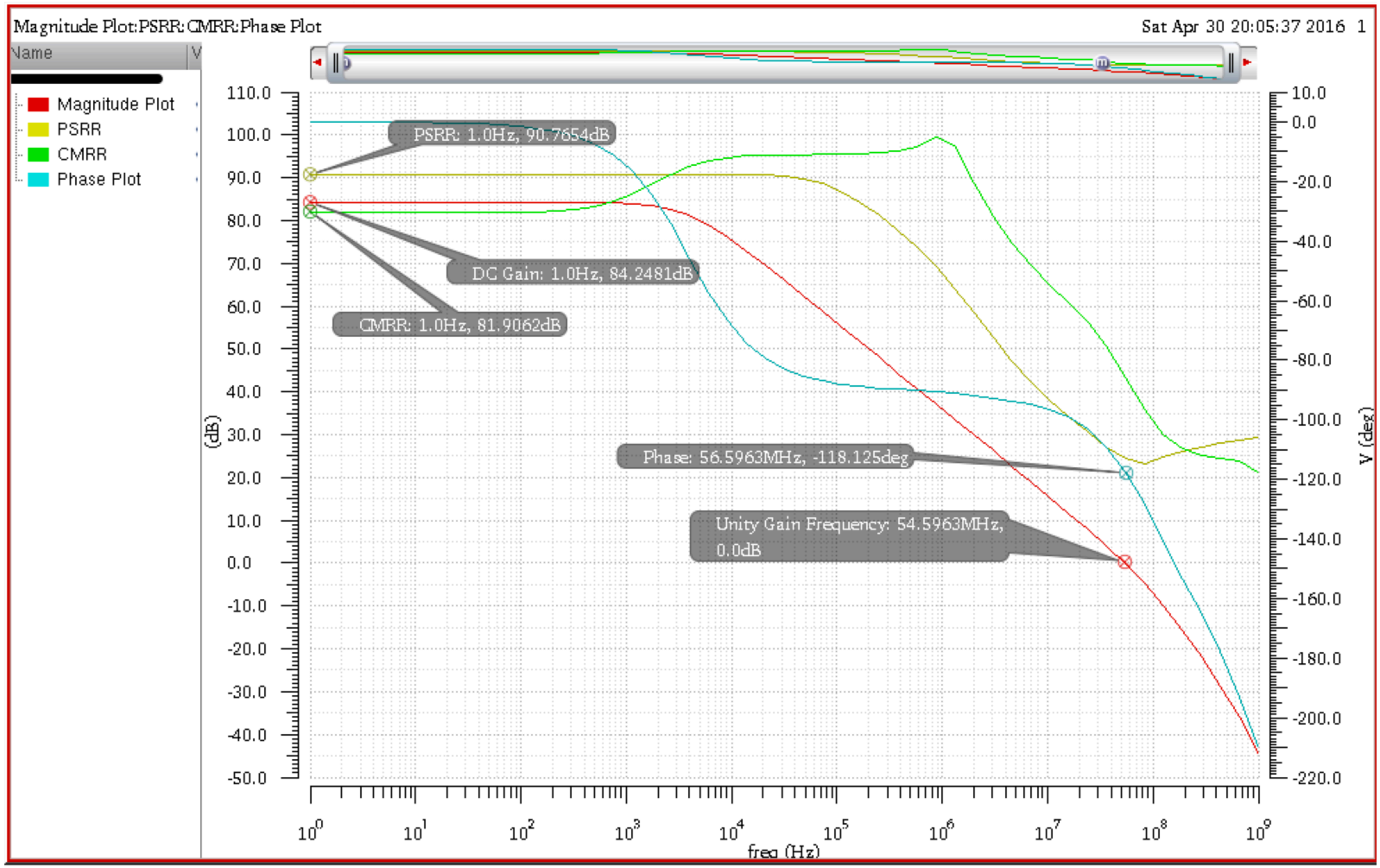


Figure 2: Higher Bandwidth Amplifier: Output at 1.55V

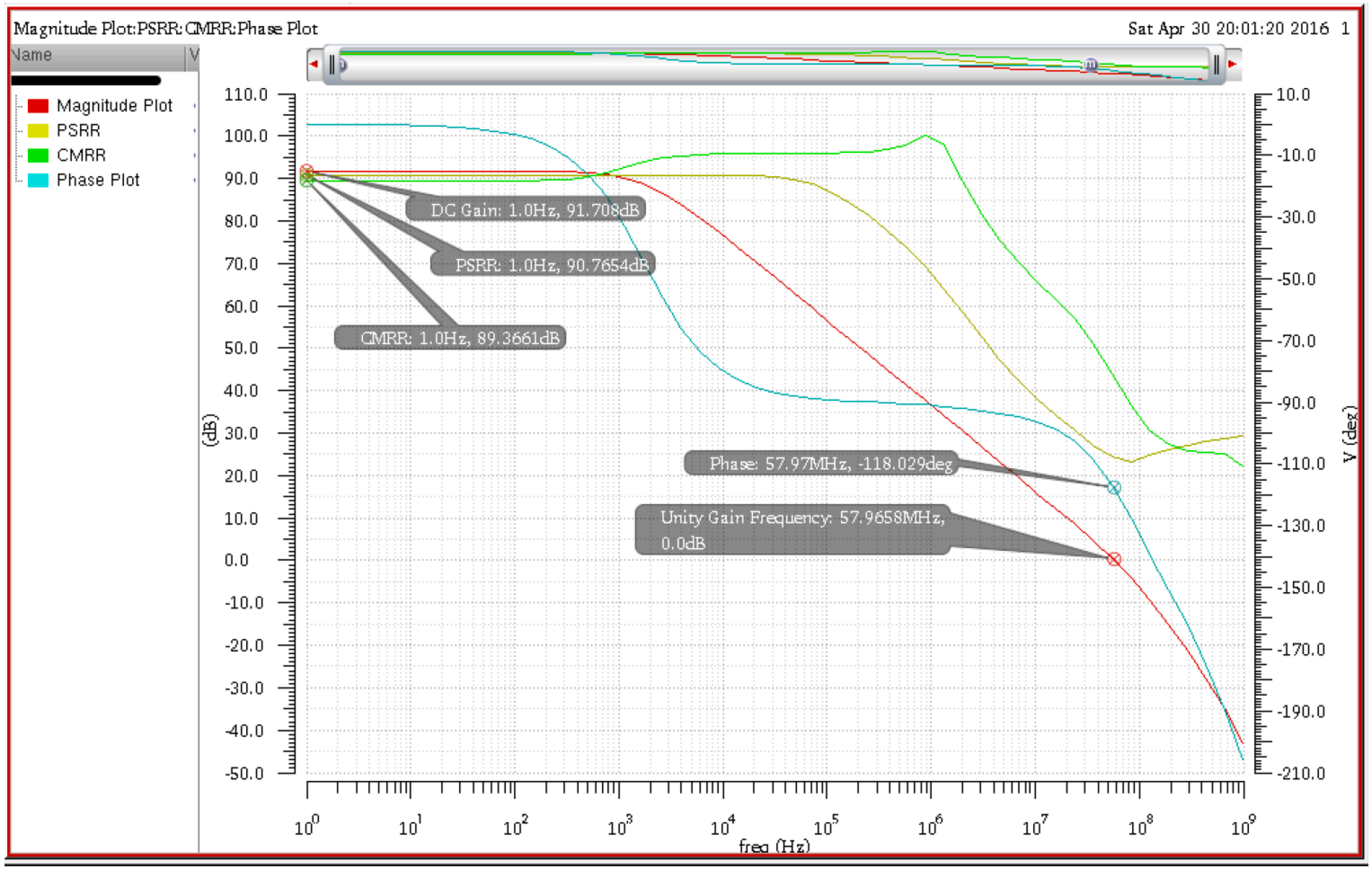


Figure 3: Higher Gain Amplifier: Output at 250mV

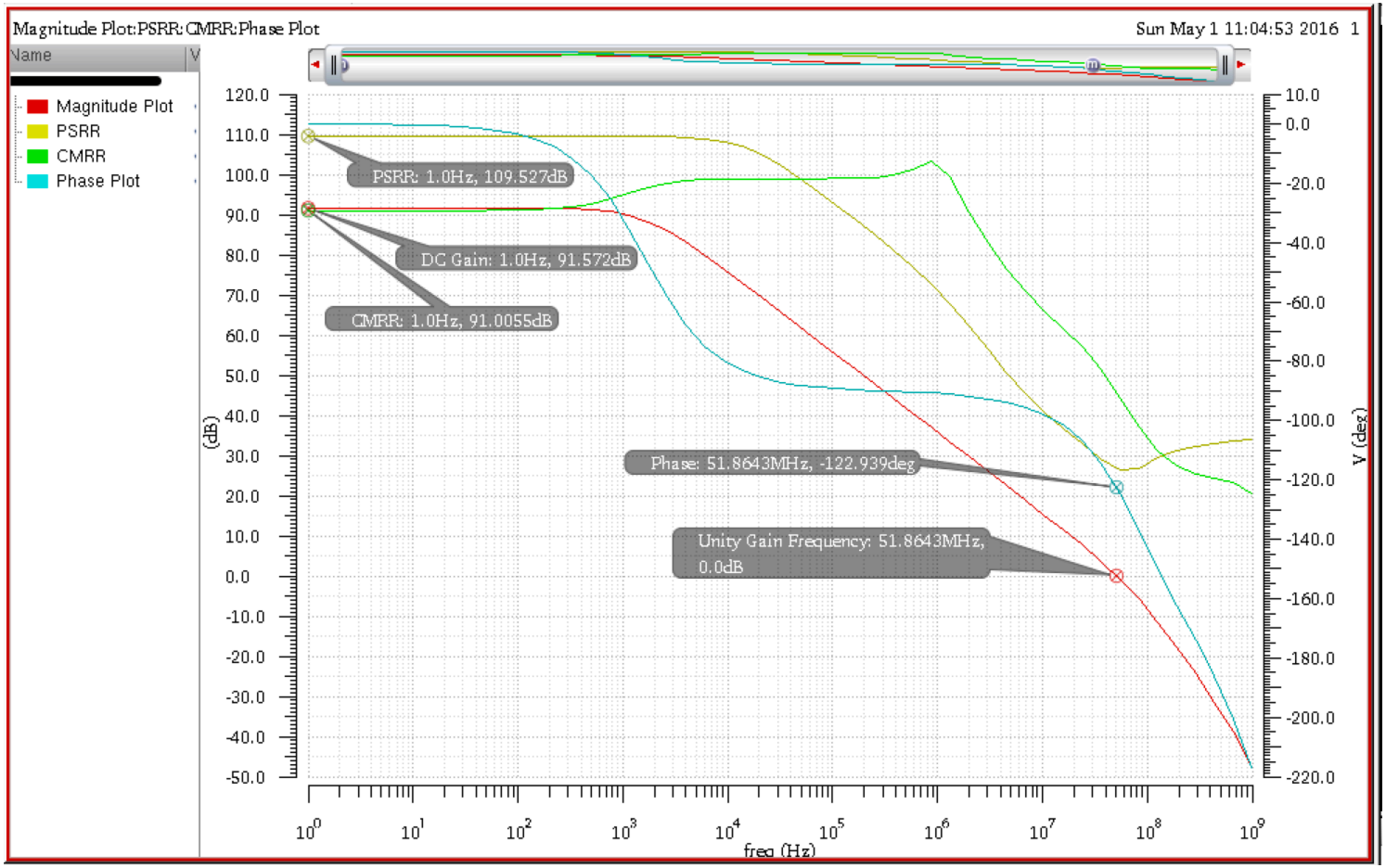
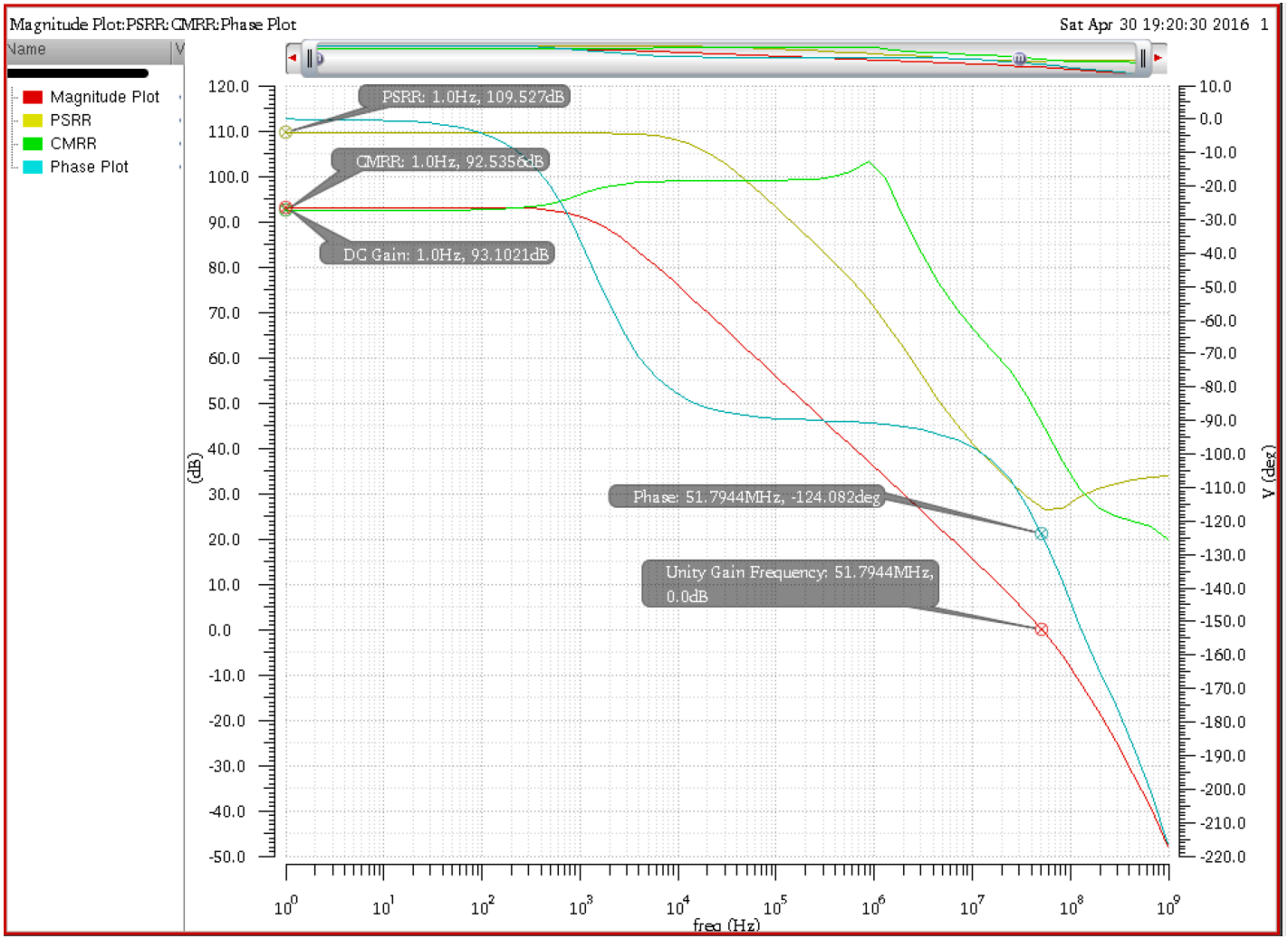


Figure 4: Higher Gain Amplifier: Output at 1.55V



5 Tables

Table 1: Specifications and Results - Higher Bandwidth Amplifier

	Specs	Units	Calculated Result	Simulation 1 (Vout = 250mV)	Simulation 2 (Vout = 1.55V)
Gain Bandwidth Product	50	MHz	50	54.59	57.96
Phase Margin	55	Degrees	56.3	61.88	61.97
Maximum Power	3	mW	2.68	2.86	2.69
Output Swing	0.25 to 1.55	V	0.2 to 1.6	0.25 to 1.55	0.25 to 1.55
DC small signal Gain	> 10 000	V/V	1,465,600	16,308	34,535
Input Voltage Range	0.9 to 1.8	V	0.9 to 2.3	0.9 to 1.6	0.9 to 1.6
Capacitive load	10	pF	10	10	10
Supply Voltage	1.8	V	1.8	1.8	1.8
CMRR	n/a	dB	n/a	81.9	89.4
PSRR	n/a	dB	n/a	90.8	90.8

Table 2: Device Parameters and DC Operating Conditions - Higher Bandwidth Amplifier

Device	W (um)		L (um)		Current Density (uA)		
						Actual	
	Predicted	Actual	Predicted	Actual	Predicted	Output 250mV	Output 1.55V
M1,M2	5.24	10	0.18	0.18	264	264	264
M3,M4	32.75	30	0.54	0.54	66	61	61
M5,M6,M7,M8	3.3	5	0.54	0.54	66	61	61
M11,M12	164	152	0.54	0.54	328	325	325
M13	26.2	20	0.54	0.54	528	527	527
M9	78.5	44	0.54	0.54	785	844	808
M10	392.5	364	0.54	0.54	785	844	808
M14, M15	n/a	.40	n/a	0.54	n/a	10	10
M16, M17	n/a	5	n/a	0.54	n/a	10.26	10.26
M19	n/a	1	n/a	0.54	n/a	10.55	10.55
M20	n/a	10	n/a	0.54	n/a	65	65
M21	n/a	3.3	n/a	0.54	n/a	65	65

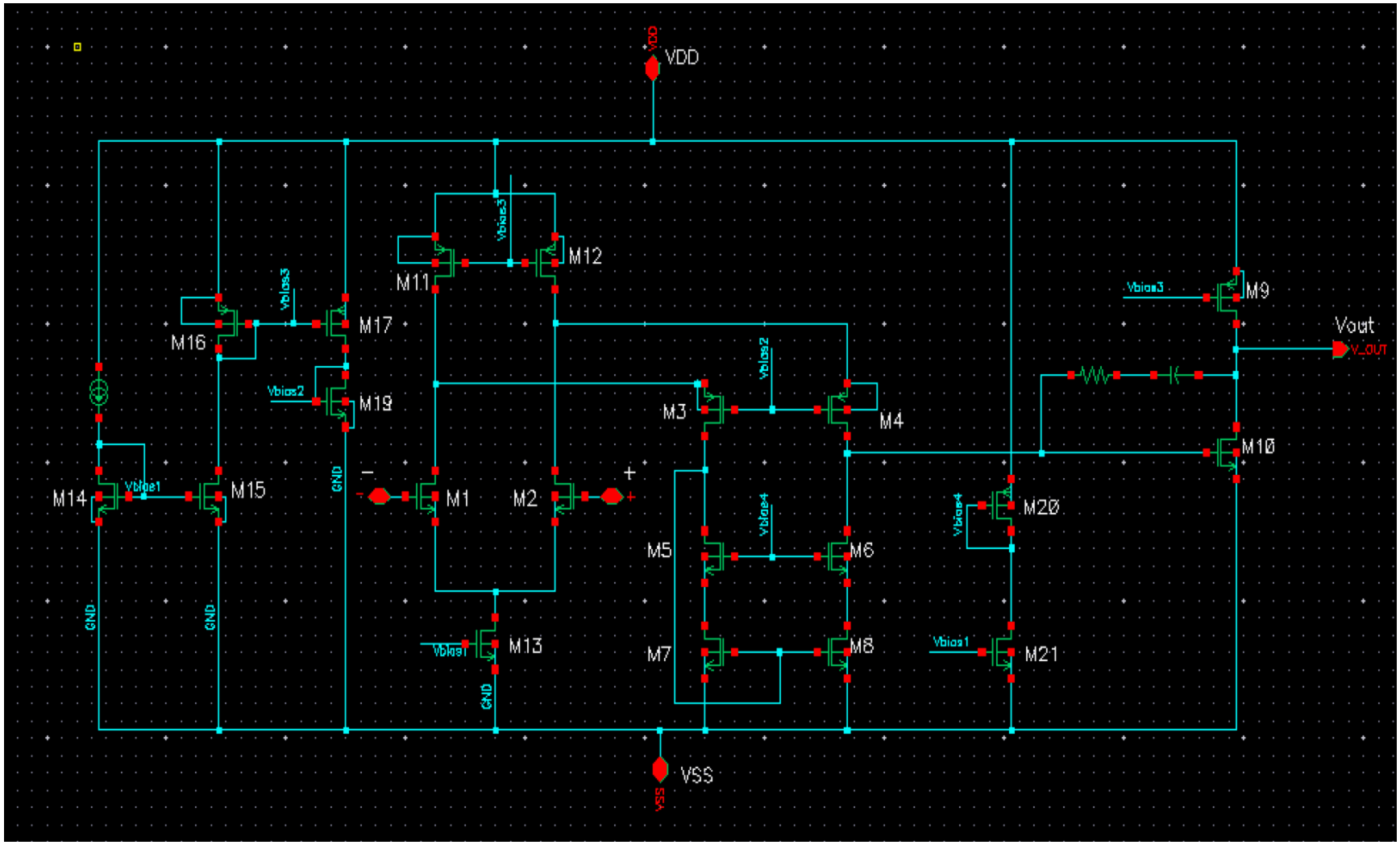
Table 3: Specifications and Results - Higher Gain Amplifier

	Specs	Units	Calculated Result	Simulation 1 (Vout = 250mV)	Simulation 2 (Vout = 1.55V)
Gain Bandwidth Product	50	MHz	50	51.86	51.79
Phase Margin	55	Degrees	56.3	57.1	55.92
Maximum Power	3	mW	2.68	2.24	2.13
Output Swing	0.25 to 1.55	V	0.2 to 1.6	0.25 to 1.55	0.25 to 1.55
DC small signal Gain	> 10 000	V/V	1,465,600	35,503	45,196
Input Voltage Range	0.9 to 1.8	V	0.9 to 2.3	0.9 to 1.55	0.9 to 1.55
Capacitive load	10	pF	10	10	10
Supply Voltage	1.8	V	1.8	1.8	1.8
CMRR	n/a	dB	n/a	91.0	92.5
PSRR	n/a	dB	n/a	109.5	109.5

Table 4: Device Parameters and DC Operating Conditions - Higher Gain Amplifier

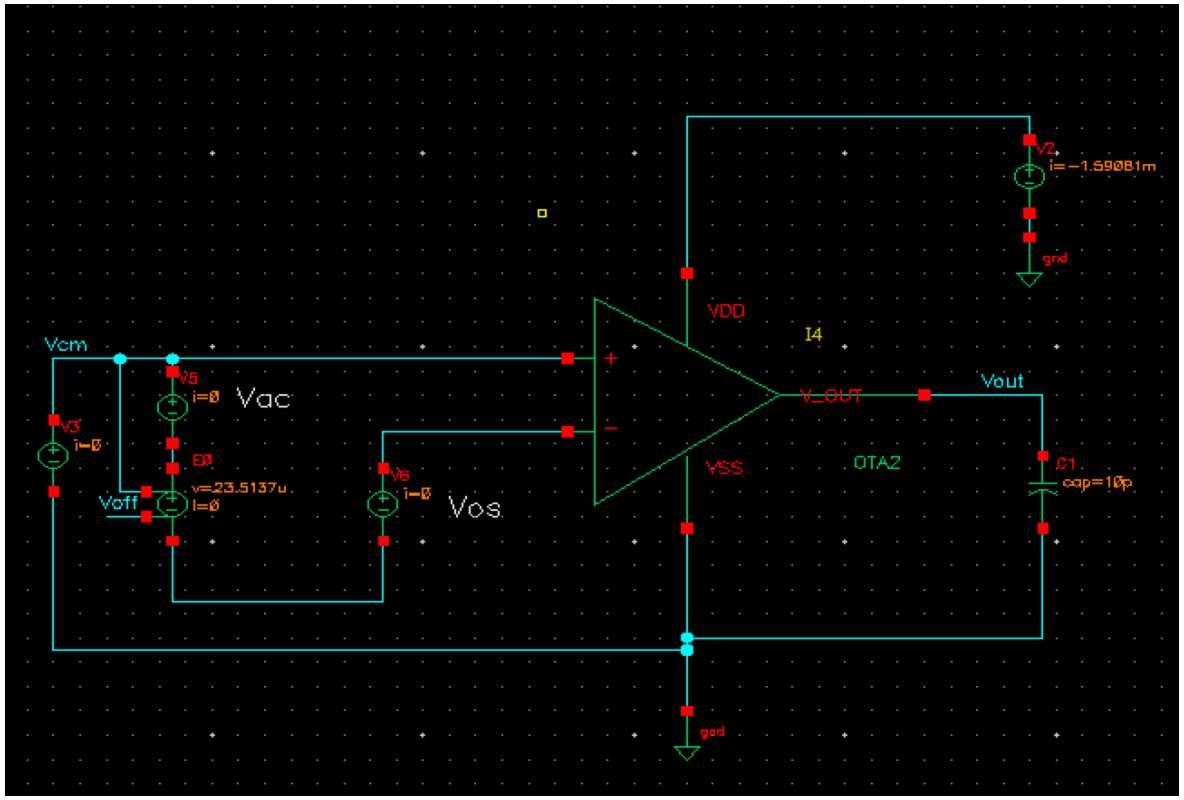
Device	W (um)		L (um)		Current Density (uA)		
	Predicted	Actual	Predicted	Actual	Predicted	Actual	
						Output 250mV	Output 1.55V
M1,M2	5.24	10	0.18	0.18	264	264	264
M3,M4	32.75	30	0.54	0.54	66	61	61
M5,M6,M7,M8	3.3	5	0.54	0.54	66	61	61
M11,M12	164	88	0.54	0.54	328	325	325
M13	26.2	20	0.54	0.54	528	527	527
M9	78.5	50	0.54	0.54	785	499	442
M10	392.5	214	0.54	0.54	785	499	442
M14, M15	n/a	.40	n/a	0.54	n/a	10	10
M16, M17	n/a	5	n/a	0.54	n/a	10.26	10.26
M19	n/a	1	n/a	0.54	n/a	10.55	10.55
M20	n/a	10	n/a	0.54	n/a	65	65
M21	n/a	3.3	n/a	0.54	n/a	65	65

6 Amplifier Schematic



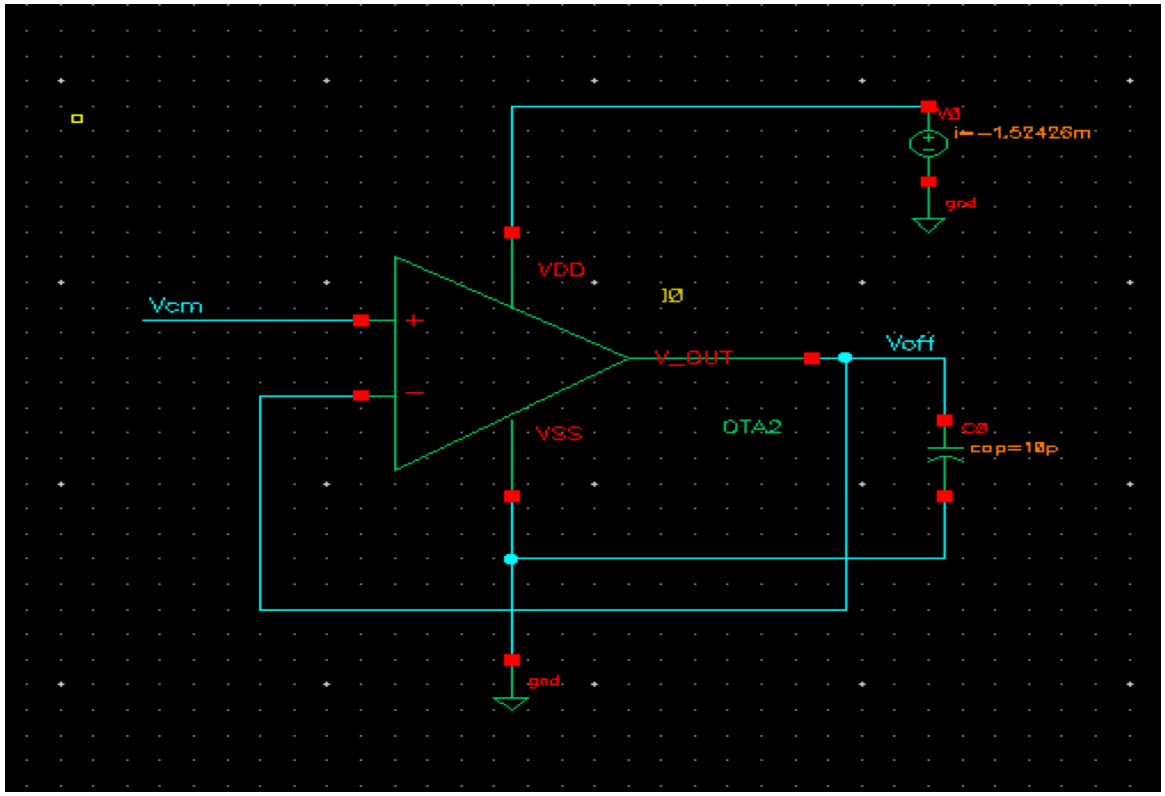
7 Test Benches

7.1 DC Gain and Bandwidth



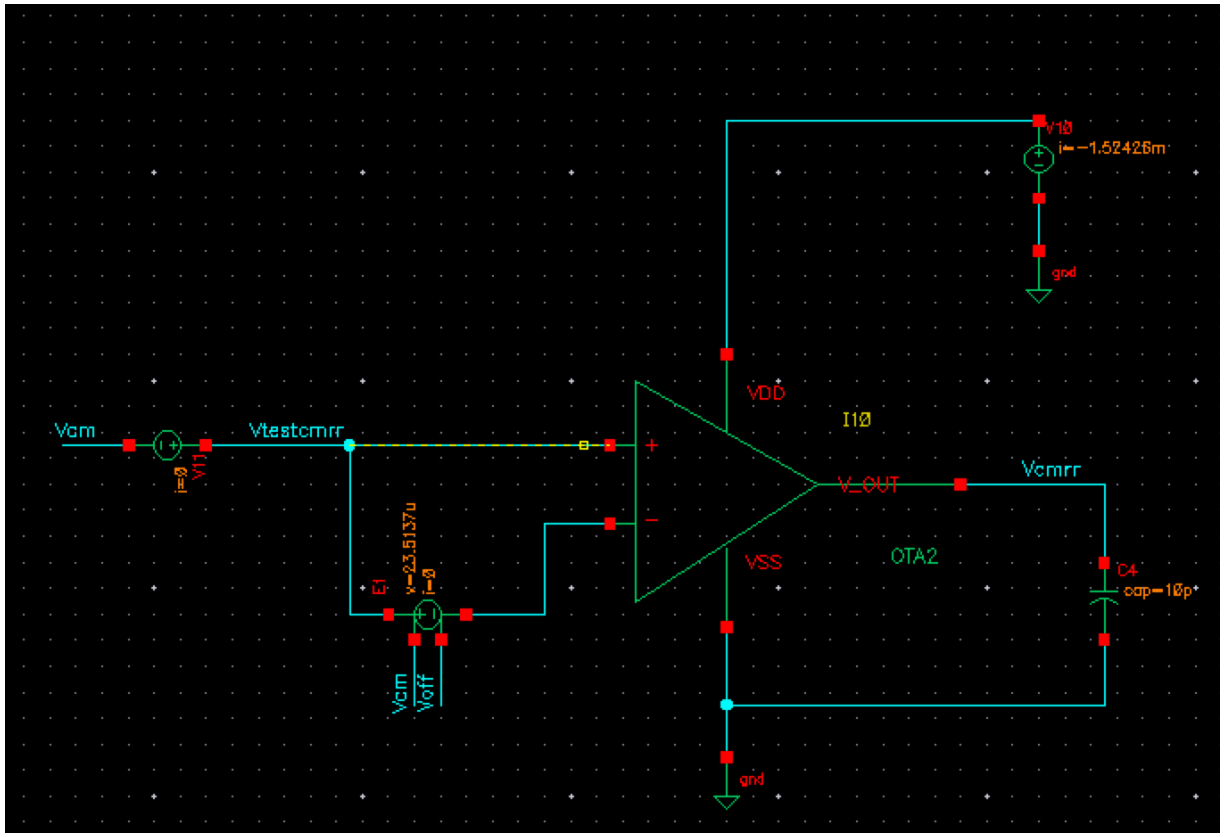
I used the above test bench to determine the Magnitude and Phase plots of my amplifier at different DC output voltages (see Figures 1-4). I tested my amplifier at the output voltages 0.25V and 1.55V in order to assure that my amplifier met specifications throughout the entire output range of the amplifier, by appropriately adjusting Vos.

7.2 Systematic Offset Voltage



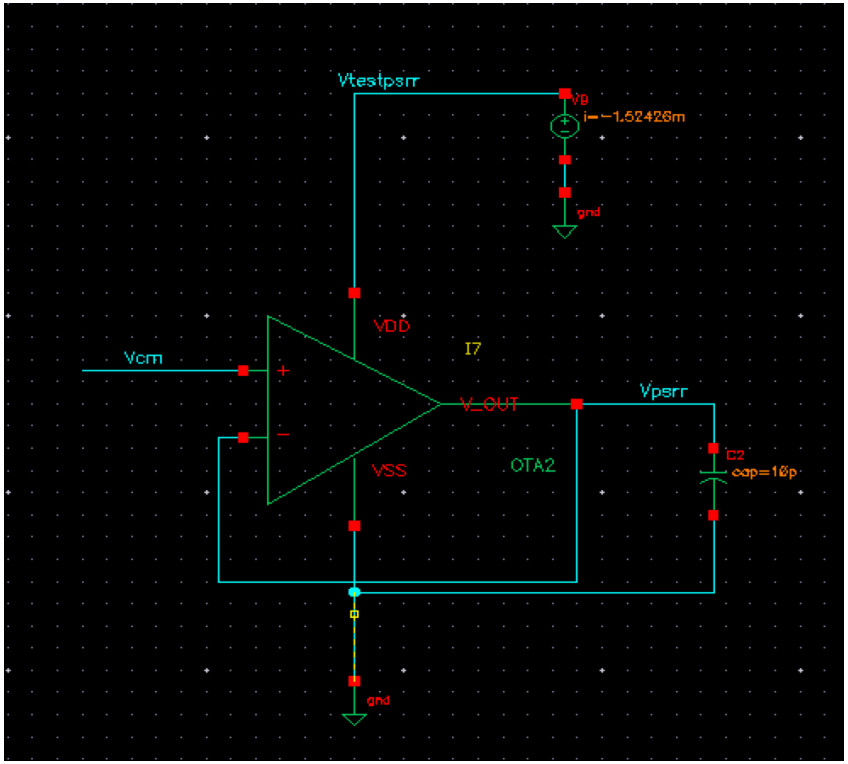
I use the above test bench to determine the systematic offset voltage of my amplifier that arises due to device mismatches that cannot be accurately predicted. I use this offset voltage in my other test benches to offset the inverting and non-inverting input terminal voltages such that the output of the amplifier does not rail during AC testing.

7.3 Common Mode Rejection Ratio



I use the above test bench to calculate the common mode rejection ratio of my amplifier. The AC signal, Vtestcmrr, is applied to both the inverting and non-inverting terminals of my amplifier, and the output voltage is compared to the input voltage to determine the common mode gain. This gain can be compared to the differential gain to determine the CMRR of my amplifier. See Figures 1-4 for plots of CMRR vs frequency.

7.4 Power Supply Rejection Ratio



I used the test bench above to determine the power supply rejection ratio (PSRR) of my amplifier. I apply a small AC signal, Vtestpsrr, to VDD of my amplifier, and compare the input signal magnitude to the magnitude of the signal at the amplifier's output to determine the gain from VDD to Vout. This gain, in dB, represents the PSRR of my amplifier. See Figures 1-4 for plots of PSRR vs frequency of my amplifier.